

More illegal MAL.

- B is assigned twice
- ALU is configured differently
- A is assigned twice

ac := ac + mbr ; BAD: B = mbr but only A = MBR

ac := mbr + ac ; OK

{ AMUX=1, ALU=0, C=AC, B=AC }
 => ac := mbr + ac; A is not assigned

1 | 00 | 00 | 00 | 0 | 0 | 0 | 0 | 1 | 0001 | 0001 | ???? | ?x0

alu := (ac + ac); c := lshift(ac + ac); OK

mbr := ac; c := lshift(ac);
 BAD { MBR=1, ALU=10, A=0001, SH=00 }
 { ALU=10, A=0001, SH=10 } ←

alu := ac; c := lshift(ac);

mar := ac; ac := AC + 1;
 BAD → B = AC → B = 1

mar := ac; ac := 1 + ac;

mar := ir; mbr := lshift(ac + ir); tir := bshift(ac + ir);

wr; if n then goto 22; alu := ac + ir;

OK: 0 | 10 | 00 | 10 | 1 | 1 | 0 | 1 | 1 | 0100 | 0001 | 0011 | 0011 0111